Shahed Enamul Quadir, Ph.D.

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EDUCATION

***University of Connecticut*,** Storrs, CT
Doctor of Philosophy in Electrical and Computer Engineering, May 2020
The University of Alabama at Birmingham, AL
Master of Science in Electrical and Computer Engineering, August 2012
***Bangladesh University of Engineering and Technology*,** Dhaka, Bangladesh
Bachelor of Science in Electrical and Electronic Engineering, March 2009

EMPLOYMENT EXPERIENCE

Assistant Professor

Midwestern State University, Wichita Falls, TX | 2026 - Present

Classes:

- Digital Signal Processing
- Control Systems
- Electronics Lab (EENG and MENG)

Assistant Professor

Monmouth College, Monmouth, IL | 2021 – 2025

- Designed and delivered undergraduate courses in engineering.

Classes Taught:

- Introduction to Engineering
- Circuit Analysis
- Electric Power Machines
- Embedded Systems
- Senior Design
- Engineering Computations with Matlab/Python
- Digital Electronics
- Statics
- CMOS VLSI Circuit Design

Post-doctoral associate

University of Florida, Gainesville, FL | 2020 –2021

- Designed digital sensors, microelectronic devices, and systems; developed *secure analog and mixed-signal circuits*.
- Worked on analog obfuscation and hardware Trojan detection using side-channel analysis to enhance circuit security and trust.

Signal Analysis and Artificial Intelligence Intern

IMCORP *(In collaboration with* ***MathWorks****),* Hartford, CT | January 2019- December 2019

- Analyzed signal data from field tests of underground power cables using IMCORP's proprietary software.
- Implemented a *curve-fitting algorithm* using MATLAB to *separate overlapping signals* to improve *the partial discharge (PD) signal resolution*.

***Graduate Research Assistant,* Storage and Network Systems Laboratory (*SNSL*) Lab**

***University of Connecticut**,* Storrs, CT | 2014 - 2020

- Designed an obfuscated key using a *Physical Unclonable Function (PUF)* of *integrated circuits (ICs),* which has been implemented in an FPGA.
- Generated *session key* using Physical Unclonable Functions (PUFs) that extract randomness from a device's physical characteristics.
- Proposed and implemented a novel PUF design based on resistor and capacitor variations for a low-pass filter (LoPUF).

Related Teaching Experience

Teaching Assistant, University of Connecticut, Storrs, CT | January 2016 - May 2020

- ECE 2000 – Electrical & Computer Engr. Principles
- PHYS1201Q – General Physics I
- PHYS1202Q – General Physics II
- PHYS1501Q – Physics for Engineers I (Currently Studio Physics)

Lecturer, North South University, Dhaka, Bangladesh | September 2013 - January 2014
Lecturer, Bangladesh University, Dhaka, Bangladesh | September 2012 - August 2013
Lecturer, IBAIS University, Dhaka, Bangladesh | May 2009 - July 2011

Graduate Research Assistant

The University of Alabama at Birmingham, AL | August 2011 - August 2012

- Designed a *Beta Multiplier Reference circuit* using *Cadence 0.13 μm* CMOS technology.
- Implemented an *Ultra-Low-Power, Low-Noise bio-amplifier*. The proposed amplifier features high gain and low input-referred noise, making it suitable for *neural recording systems*.
- Designed a *low-noise operational transconductance amplifier (OTA)* in Cadence 0.13 μm CMOS technology.

SELECTED PUBLICATIONS

Journal Publications:

Published:

- M. S. Alam, ***S. E. Quadir***, et al., "*Hardware and Cyber Vulnerabilities in Embedded Systems: An Overview for Power Grids, PV, EVs and Storage Systems,*" IEEE Access, 2025.
- ***S. E. Quadir*** and J. Chandy, "*Integrated Circuit Authentication Based on Resistor and Capacitor Variations of a Low Pass Filter (LoPUF)*." International Journal of High-Speed Electronics and Systems, International Journal of High-Speed Electronics and Systems, 2022. 31, 01n04.
- ***S. E. Quadir*** and J. Chandy, "*Key Generation for Hardware Obfuscation Using Strong PUFs*." Cryptography, MDPI, 3(3), 17, 2019.
- ***S. E. Quadir*** and J. Chandy, "*Low Pass Filter PUF: Authentication of Printed Circuit Boards Based on Resistor and Capacitor Variations*." International Journal of High-Speed Electronics and Systems, 27. 03n04, 2018.
- ***S. E. Quadir***, J. Chen, et al., "*A Survey on Chip to System Reverse Engineering*." ACM Journal on Emerging Technologies in Computing Systems (JETC), 2016.

Conference Publications:

- S. Alam, ***S. E. Quadir***, et al., "*A Review of Hardware-Based Security Techniques for Cyber-Physical Power Systems,*" Interdisciplinary Conference on Electrics and Computer (INTCEC), IEEE, 2025.
- ***S. E. Quadir*** and J. Chandy, "*Embedded Systems Authentication and Encryption Using Strong PUF Modeling*," IEEE International Conference on Consumer Electronics (ICCE), 2020.
- N. Asadi, ***S. E. Quadir***, et al., "*Rapid Nondestructive Reverse Engineering* of *Printed Circuit Boards* by High-Resolution X-ray Tomography," GOMACTech, 2015.
- ***S. E. Quadir***, et al., "*A Low-Power Low-Noise Bioamplifi*er for *Multielectrode Neural Recording Systems,*" IEEE International Symposium on Circuits and Systems (ISCAS), Seoul, Korea, May 20-23, 2012.

Poster Presentations:

- Thomas Henson, Braeden Brauman, Turner Plumer, and ***S. E. Quadir***, "*Embedded Systems for Community Solutions: Programming with the MSP430*," Monmouth College Scholars' Day, 2025.
- X. Borst, P. Rousey, C. Stasko, and ***S. E. Quadir***, "*Creating a Physical Unclonable Function using Multiplexers, Counters, Comparators, and a Ring Oscillator Chain*," Connecticut Symposium on Microelectronics & Optoelectronics, 2024 (Best Poster Award).
- I. Gustafsson, B. Brauman, ***S E. Quadir***, and C. Fasano, "*Detection of Counterfeit Electronic Components Using a Simple Circuit*, " Bulletin of the American Physical Society, 2023.
- ***S. E. Quadir*** and J. Chandy, "*Logic Obfuscation and Design Locking for Secured ICs*," Connecticut Symposium on Microelectronics & Optoelectronics, 2019 (Best Poster Award).
- ***S. E. Quadir*** and J. Chandy, "*Electronic Authentication using a Low Pass Filter PUF*." CMOC 2018.
- ***S. E. Quadir***, D. Forte, and M. Tehranipoor, "*Chip to System Reverse Engineering*," CHASE Workshop 2014.

SELECTED GRADUATE PROJECTS

- Implemented a high-speed 8-bit pipelined analog-to-digital converter (ADC) in the Cadence 0.13 μm CMOS process. Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) are also calculated and simulated.
- Optimized physical design and verified timing and power analysis of a DRAM controller with the Xilinx ISE design suite.
- Designed a 4X4 Multiplier in a 0.13um technology node using Cadence. The schematic and layout are verified using Cadence Diva LVS and DRC tools.
- Analyzed Short-time Fourier Transform (STFT) and Wavelet Transform (WT) on sea life and financial data to find out the features of the signals using MATLAB.
- Detected Hardware Trojan in Ring Oscillator Network (RON) using Support Vector Machine and K-center Clustering.

AWARDS AND HONORS

- Engineering lab development funding, Monmouth College
- Predoctoral Fellowship, University of Connecticut- 2017, 2018, 2019
- Merit Scholarship and Technical Scholarship, Bangladesh University of Engineering and Technology

INSTITUTIONAL & PROFESSIONAL SERVICE

- ABET Committee at Monmouth College.
- Serve on college committees, including Engineering Curriculum, Assessment, and Student Activities & Success.

- Participated in faculty development workshops on community-based pedagogy and vocation in undergraduate education.
- Peer reviewer for journals: Springer Nature Computer Science (2022–), Elsevier Microelectronics Journal (2019–), Elsevier Journal of Parallel and Distributed Computing (2020–), and ACM TODAES (2020–).
- Provided local support during CHASE workshops (2016, 2017) at the University of Connecticut.
- Member of IEEE and ASEE

RESEARCH INTERESTS

- Hardware Security and Trust: Security primitives and authentication protocols of ICs, PCBs, and cyber-physical systems (smart grids and renewable energy infrastructure).
- SoC Security: Analysis of vulnerabilities in SoC, obfuscated key, and security-aware SoC design flow.
- Supply Chain Security: IP/IC piracy prevention, digital watermarking, hardware Trojan detection, Physical Unclonable Function for key generation, and detection of counterfeit IC.
- AI and ML Applications: Hardware security, energy systems optimization, and predictive maintenance.

PROFESSIONAL TOOLS & LANGUAGE EXPERTISE

Languages and Development Tools: Verilog, VHDL, MATLAB, Mathematica, Simulink, Arduino, Raspberry Pi, Assembly Language, Python, C / C++, Code Composer Studio (CCS), MSP430 LaunchPad (TI)
Circuit Simulation Tools: Cadence: Virtuoso Layout Editor, Cadence Allegro PSpice Simulator, HSPICE, Synopsys ICC, Synopsys Design Compiler, LabVIEW, VCS, PrimeTime, ModelSim
FPGA Design: Xilinx ISE, Vivado Design Suite, FPGA Editor
CAD Tools and related Software: Fusion 360, SolidWorks, Ultimaker Cura (3D printing Slicer)
Debugging: Logic Analyzer, Oscilloscopes, Spectrum Analyzer, ChipScope Pro
Operating Systems: Linux, Mac OS, and Microsoft Windows
Scripting Language: TCL, Perl Script, and Bash, and **Standard Architecture:** RISC / MIPS (32 bits)

VOLUNTEER EXPERIENCE

- Supported student recruitment and outreach at Monmouth College. Served as a volunteer during first-year student registration.
- Regularly meet with prospective students and their families to discuss the Engineering program and provide them with tours of our department's facilities.
- Represented the Bengali language at Monmouth College's award-winning Classics Day, engaging hundreds of students and guests from across the Midwest.
- Provided regular tutoring in physics at the Physics Learning Resource Center (PLRC), University of Connecticut, to support students with homework and conceptual understanding.
- Volunteered as a math tutor for the Student Support Services (SSS) summer program at UConn and assisted first-generation college students with foundational concepts.