SYLLABUS
EENG 3154: Integrated Circuit Design
(Required Course - Fall 2024)

COURSE INSTRUCTOR
Dr. Yuyao Wang

LAB INSTRUCTOR
Dr. Yuyao Wang

COURSE & LAB SCHEDULE

Days	*Time*	*Location*
Monday	11:00 am – 11:50 am	MY 131
Tuesday		
Wednesday	11:00 am – 11:50 am	MY 131
Thursday		
Friday	11:00 am – 11:50 am	MY 131
Friday*	1:30 pm – 03:20 pm	MY 140

**Lab sessions are indicated with an asterisk.*

OFFICE HOURS

Days	*Time*	*Location*
Monday	3:00 pm – 5:00 pm	MY 127
Tuesday		
Wednesday	3:00 pm – 5:00 pm	MY 127
Thursday	3:00 pm – 4:00 pm	MY 127
Friday		

MSU CATALOG DESCRIPTION
This course provides a broad range of topics from CMOS technology, static CMOS design to dynamic logic design and pass transistor logic. It also provides students with an in-depth understanding of digital VLSI design and simulation through the utilization of a Field Programmable Gate Array (FPGA) board and Verilog HDL programming. It covers theoretical foundations and practical experiments by focusing on understanding Verilog programming with different modelling styles such as gate, dataflow, and behavioral models. The practical laboratory sessions involve hands-on programming with Verilog HDL programming using Intel Quartus Prime Lite and Intel MAX10 FPGA DE 10-Lite board to explore the full VLSI design course, from the initial design to the hardware implementation level.

COURSE PRE-REQUISITES
MENG 2204: ELECTRONICS DEVICE

Course Resources:
• Hardware: Intel Max10 FPGA DE 10-Lite Development Boards.
• Software: Intel Quartus Prime Lite Design Software.

TEXTBOOK
"Digital Design with RTL Design, VHDL, and Verilog", *Frank Vahid,* John Wiley & Sons Inc.

SUPPLEMENTAL MATERIAL
CMOS VLSI Design: A Circuits and Systems Perspective (4th Edition), *Weste, Neil, Harris, David*, Addison-Wesley.
Charles H. Roth, Jr. Lizy Kurian John, Byeong Kil Lee, Digital Systems Design Using VERILOG, Cengage Learning, 2014.

LIST OF TOPICS COVERED

• Number systems and Boolean algebra	• Other Logic Styles
• Logic optimization	• Design Flow with Verilog-HDL
• Inverter Characteristics	• Combinational Logic Design with Verilog
• Static CMOS Logic Design	• Sequential Logic Design with Verilog
• Gate sizing and Noise Margin	• Writing Testbench

Additional material may be covered as time permits.

SPECIFIC GOALS OF INSTRUCTION

Table 1: A detailed list of course objectives matched with the ABET outcomes (1-7).

	ABET OUTCOMES*						
COURSE OBJECTIVES	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Ability to analyze and design static CMOS logic (hw, lab, exam)	**X**					**X**	**X**
Ability to calculate circuit delay and noise margin (hw, lab, exam)	**X**					**X**	**X**
Ability to apply gate sizing for circuit optimization (hw, lab, exam)	**X**					**X**	**X**
Ability to perform logic design with other logic styles (hw, lab, exam)	**X**					**X**	**X**
Ability to design combinational logic circuits with Verilog-HDL (hw, lab, exam)	**X**					**X**	**X**
Ability to design sequential logic circuits with Verilog-HDL (hw, lab, exam)	**X**					**X**	**X**
Ability to design Finite State Machine with Verilog-HDL (hw, lab, exam)	**X**					**X**	**X**
Ability to write testbench for digital logic (lab)	**X**					**X**	**X**
Ability to implement and debug digital systems on FPGA platforms (lab)	**X**					**X**	**X**

*__Table 2:__ Detailed descriptions of the ABET outcomes (1-7) listed in Table 1.

ABET Outcome	**DESCRIPTION**
1	an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics.
2	an ability to apply engineering design to produce solutions that meets specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors.
3	an ability to communicate effectively with a range of audiences.
4	an ability to recognize ethical and professional responsibilities in engineering situations and make informed judgements, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts.
5	an ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives.
6	an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions.
7	an ability to acquire and apply new knowledge as needed, using appropriate learning strategies.

COURSE ORGANIZATION AND STUDENT PERFORMANCES ASSESSMENT

- Lecture Format

This course consists of three 50-minutes sessions per week. The class will be spent mostly explaining and discussing concepts and designing example digital logic systems. Lectures will not be used to communicate the entire textbook course content and thus students should focus on the topics covered in the class.

- Attendance
  Attendance is required for each student. Absences of more than five lectures without proofs of legitimate excuses will result in a failing grade. **For each absence without proofs of acceptable excuses there will be 1 point off from Attendance & Class performance. If you are over 30 minutes late for the class, you are still allowed to sit in the class, but 1 absence will be counted.**

- Student Attitude
  Once class starts, the use of cell phones, reading of newspapers, conducting private discussions, using the computer (unless requested by the instructor), working on anything that is not directly related to the course, and making derogatory remarks about your classmates or instructor will not be accepted and may result in your dismissal from the class. **Each time you are caught will result in 1 point off from Attendance & Class performance. Total grade for Attendance & Class performance is 5 points at beginning and it could become negative.**

- Homework
  Homework will be assigned based on covered topics. It will be turned in each week, unless specified by the instructor. **Homework must be turned in at the beginning of class. Once class starts, late homework will be graded 80% of the full grade. If you arrived late, your homework will also be counted as late. Late homework will only be accepted until the end of due day.** However, if you copied from your classmates, you would receive zero points.

- Exams
  There will be two regular exams: one midterm exam and one final exam. Exam will be closed book and cheat sheet is not allowed. **Each exam is based on the course materials developed between two consecutive exams and possibly lab material if exist.** Students are expected to take the exam on the scheduled date and time it is given. However, if for some acceptable reason the student is not able to do so, then he must inform the instructor in advance in writing. The instructor will then decide whether he will be allowed to take a makeup exam, depending on the validity of his excuse. There is only one chance for makeup exam no matter what.

- Evaluation Method
  Your performance will be tested regularly throughout the semester by exams and homework assignments. There will be two exams. While homework assignments may contain a number of problems, it may be the case that only a subset of problems will be graded. However, you must attempt all problems. Do not try to guess which (if any) problems will not be graded.

- Midterm Progress Report
  In order to help students keep track of their progress, a Midterm Progress Report will be provided for each at-risk student through WebWorld. The grades reported will not be reflected on the students' transcript; nor will they be calculated in the cumulative GPA. However, at-risk students should put more effort and seek out tutoring.

- Course Grade

Midterm	Oct	20%
Labs		25%
Homework		20%
Attendance & Class performance		5%
Final Exam	Dec	30%

***Bonus point in any case will only apply to those with a final grade lower than C.**

GENERAL GUIDELINES

- Plan on spending at least 5 hours outside of class to study the material and to work on homework assignments, and lab experiments. Do not wait until the last day to start working on your assignment, or prepare for the exam.
- Utilize the office hours throughout the semester to seek explanations whenever you have questions.
- In engineering, neatness is a must, not a luxury. Be advised that you will be penalized for lack of neatness.
- You are encouraged to study in group but have to write your own homework.
- Generative AI can assist with understanding theories but approach its answers with caution. Do not rely on AI for hardware design or homework, as it may provide incorrect information, and you will be responsible for any resulting penalties.

CONFLICT RESOLUTION

a. The student should contact the instructor face to face or via e-mail if there is an issue with the course or the instructor. The faculty and the student will discuss this face to face or via email. Hopefully, a resolution is reached on the issue.

b. The student should notify the faculty via email again if the issue still did not get resolved after the first encounter or communication.

c. The student can then contact the Chair of the McCoy School of Engineering, Dr. Desai, face to face or via email, (raj.desai@msutexas.edu), and discuss this issue. Dr. Desai will discuss the issue at hand with the faculty member. Dr. Desai will discuss the result of this discussion with the student. Hopefully, a resolution is reached on the issue after this.

d. The student should notify the Chair via email if the issue still did not get resolved.

e. The Chair will contact the Dean and try to resolve the conflict. In case the conflict deals with the student grade, she will forward the case to the Grade Appeals Committee if necessary.

GENERAL EDUCATION STATEMENT

Students in this course must demonstrate their competency in oral and written communication through written project tasks assignments. They must also demonstrate their ability to use the English language.

ACADEMIC INTEGRITY POLICY

Scholastic dishonesty will not be tolerated and will be prosecuted to the fullest extent. You are expected to have read and understood the current issue of the student handbook regarding student responsibilities & rights, and the intellectual property policy information about procedures and what constitutes acceptable on-campus behavior. Any form of plagiarism will not be accepted and will be heavily reprimanded.

DISABILITY SUPPORT SERVICES

Students registered with Disability Support Services should have a letter verifying their disability and the appropriate accommodations.

DISCLAIMER STATEMENT

Information contained in this syllabus, other than grading, late assignments, and attendance policies, may be subject to change with advance notice, as deemed appropriate by the instructor.